Lab 02 - First Verilog

In this lab, you’ve learned how to do an initial and simple design in Verilog to learn the Vivado tooling and process involved in RTL/FPGA design.

# Rubric

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| --- | --- | --- |
| **Item** | **Description** | **Value** |
| Summary Answers | Your writings about what you learned in this lab. | 25% |
| Question 1 | Your answers to the question | 25% |
| Question 2 | Your answers to the question | 25% |
| Question 3 | Your answers to the question | 25% |

# Lab Summary

I learned how to create a new project in Vivado. I learned how to run said project as a simulation. I learned how to connect parts to my computer to display said project, in this project my partner and I used a board. I learned how to write code connecting LEDs and switches on a board.

# Lab Questions

## 1 - Describe the stages of building a Verilog project in Vivado.

Step #1: Open Vivado and press the Create New Project link

Step #2: Name your project

Step #3: Select your project type

Step #4: Add the correct files

Step #5: Customize said files

Step #6: Add constraints

Step #7: Select needed board and/or parts

Step #8: Hit Finish to create your new project

## 2 - What is the value in looking at the elaborated design schematic?

A design schematic puts words into a picture. It can help recognize how to build the schematic but also recognize future errors.

## 3 - Why should we simulate our designs frequently? What does the simulation do?

A simulation displays a computed form of our design. Simulating our designs frequently is like running code frequently, the more we do it as it changes the higher likelihood we catch errors and the easier time it is for us to fix said errors.

# Code Submission

Upload a .zip of all your code or a public repository on GitHub.